REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-71 are presently pending in this application, Claims 12-71 having been withdrawn from further consideration by the Examiner, Claims 1-11 having been amended by the present amendment.

In the outstanding Office Action, Claims 1, 2, 6-8 and 10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Takeuchi et al. (U.S. Publication 2002/0127418) in view of Kanber (U.S. Patent 5,312,765); Claims 3 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Takeuchi et al. and Kanber in view of Lee et al. (U.S. Patent 5,452,283); Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Takeuchi et al. and Kanber in view of Stone (U.S. Patent 5,530,288); and Claims 5 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Takeuchi et al. and Kanber in view of Lee et al. and Stone.

Claims 1-11 have been amended to clarify the subject matter recited therein and also to correct improper multiple dependencies. These amendments are believed to find support in the specification, claims and drawings as originally filed, and no new matter is believed to be added thereby. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language.

Before addressing the rejections based on the cited references, a brief review of Claim 1 as currently amended is believed to be helpful. Claim 1 is directed to a substrate for mounting an IC chip and recites "an insulating substrate having a first surface and a second surface on an opposite side of the first surface; a first built-up structure formed on the first surface of the insulating substrate and comprising a conductor circuit and an interlaminar

insulating layer; a second built-up structure formed on the second surface of the insulating substrate and comprising a conductor circuit and an interlaminar insulating layer; a first solder resist layer formed as an outermost layer over the first built-up structure; a second solder resist layer formed as an outermost layer over the second built-up structure; an optical element mounted over the first solder resist layer; and an optical path for transmitting optical signal to or from the optical element and penetrating through the insulating substrate, first built-up structure, second built-up structure, first solder resist layer and second solder resist layer."

The Office Action states that Claim 1 is unpatentable over Takeuchi et al. and Kanber. However, it is respectfully submitted that neither Takeuchi et al. nor Kanber teaches or suggests "an optical path for transmitting optical signal to or from the optical element and penetrating through the insulating substrate, first built-up structure, second built-up structure, first solder resist layer and second solder resist layer" as recited in amended Claim 1. Instead, Takeuchi et al. merely shows embedding electronic parts such as chip capacitors, chip inductors and chip resistance in the inside of a substrate,[1] and Kanber is directed to a method of fabricating three dimensional GaAs microelectronic device and simply describes a semiconductor device in which a microelectronic device 16 is buried in a semi-insulating substrate 10 such as GaAs and covered with a dielectric overlay layer 86 and a hollow via is formed through the semi-insulating substrate 10.[2] Therefore, the structure recited in amended Claim 1 is clearly distinguishable from Takeuchi et al. and Kanber.

Lee et al. and Stone are cited for an optical path having a vacancy and a resin composition and an optical path having a vacancy and a conductor layer around the vacancy, respectively, and are not believed to teach or suggest "an optical path for transmitting optical

[1] See Takeuchi et al., paragraph [0002].
[2] See Kanber, column 2, line 64, to column 3, line 6, column 6, lines 18-44, and Figures 11 and 12.

signal to or from the optical element and penetrating through the insulating substrate, first built-up structure, second built-up structure, first solder resist layer and second solder resist layer" as recited in amended Claim 1. Thus, the structure recited in amended Claim 1 is believed to be distinguishable from Lee et al. and Stone.

Because none of Takeuchi et al., Kanber, Lee et al. and Stone discloses the optical path as recited in Claim 1, their teachings even in combination are not believed to render the structure recited in Claim 1 obvious.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 2-11 depend directly or indirectly from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 2-11 are believed to be allowable as well.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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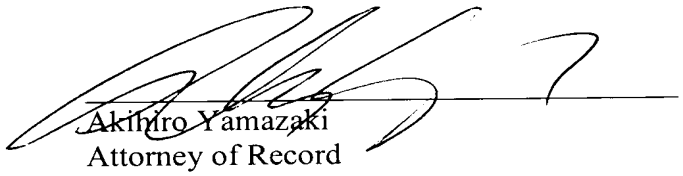

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